NVIDIA Jetson Nano Developer Kit Carrier Board P3449_B01

Specification

SP-09732-001_v1.1 | January 2020

Document History

SP-09732-001_v1.1

Version	Date	Description of Change
1.0	November 13, 2019	Initial Release
1.1	January 7, 2020	• Added Pin 1 indicators where needed in Figure 1-4 • Updated green and yellow LED cathodes description in Table 2-4

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Chapter 1. Introduction

NVIDIA® Jetson™ developer kits include a non-production specification Jetson module attached to a reference carrier board. Together with JetPack SDK, Jetson developer kits are used to develop and test software for your use case. Jetson developer kits are not intended for production use.

This specification contains recommendations and guidelines for engineers to follow to create modules for the expansion connectors on the NVIDIA® Jetson Nano™ Developer Kit carrier board as well as understand the capabilities of the other dedicated interface connectors and associated power solutions on the platform.

> **!** CAUTION:
>
> ALWAYS CONNECT JETSON NANO and ALL EXTERNAL PERIPHERAL DEVICES BEFORE CONNECTING THE POWER SUPPLY TO THE DC POWER JACK. Connecting a device while powered on may damage the developer kit carrier board, Jetson Nano, or peripheral device. In addition, the carrier board should be powered down and the power removed before plugging or unplugging devices or add-on modules into the headers. Wait for the red power VDD_IN LED to turn off. This includes the Jetson Nano module, the camera connector, the M.2 connector, and the other expansion headers.
>
> The NVIDIA Jetson Nano developer board contains ESD-sensitive parts. Always use appropriate anti-static and grounding techniques when working with the system. Failure to do so can result in ESD discharge to sensitive pins, and irreparably damage your Jetson Nano board. NVIDIA will not replace units that have been damaged due to ESD discharge.

The Jetson Nano reference carrier board is ideal for software development within the Linux environment. Standard connectors are used to access Jetson Nano features and interfaces, enabling a highly flexible and extensible development platform. Go to https://developer.nvidia.com/jetpack for access to software updates. The developer SDK includes an OS image that you will load onto your Jetson Nano device, libraries and APIs, supporting documentation, and code samples to help you get started.

1.1 Jetson Nano Feature List

- CPU and GPU
  - Quad-core Cortex-A57 complex
  - NVIDIA Maxwell™ architecture GPU
- Memory
  - 4GB LPDDR4-3200
  - 4MB QSPI-NOR (boot device)
  - Micro SD Card socket (storage)
- Multimedia
  - Ultra-low power audio processor
  - Multi-standard Video/JPEG Decoder/Encoder
- Network
  - 10/100/1000BASE-T Ethernet
- Advanced power management
  - Dynamic voltage and frequency scaling
  - Multiple clock and power domains

1.2 Carrier Board Feature List

- Connection to Jetson Nano
  - 260-pin SO-DIMM Connector
- USB
  - USB 2.0 Micro B (Device only)
  - USB 3.0 Hub to 4x Type A (Host only)
- Wired Network
  - Gigabit Ethernet (RJ45 Connector w/PoE and LEDs)
- Display
  - Stacked Connector
    - HDMI™ Type A
    - VESA® DisplayPort®
- Camera Connectors
  - 2x 15-position Flex Connectors
  - Each connector supports 2 CSI lanes
  - Camera CLK, I2C, and Control

- M.2 Key E Connector
  - PCIe x1 lane, USB 2.0
  - I2S, UART, I2C
  - Control
- Expansion Header
  - 40-pin (2x20) header
  - I2C (x2), SPI (x2), UART
  - I2S, Audio Clock, GPIOs, PWMs
- UI and Indicators
  - Automation Header: Power, Reset and Force Recovery
  - LEDs: Main Power input (VDD_IN)
- Debug/Serial
  - Serial Port Signals (on Automation Header)
- Miscellaneous
  - Fan Connector: 5V, PWM and Tach
- Power
  - DC Jack: 5.0V
  - Main 3.3V Supply: MP1475DJ
  - Main 1.8V Supply: TLV70018
  - USB VBUS Supplies: TPS259530DSG (x2)
  - HDMI Power Switch: APL3552ABI-TRG
- Developer Kit Operating Temperature Range
  - 0 ^{0}C to 35 ^{0}C (see Note)

Note: Refer to the *Jetson Nano Thermal Design Guide*

1.3 Jetson Nano Carrier Board Block Diagram

Figure 1-1 through Figure 1-5 show the block diagram and various placement views for Jetson Nano and the carrier board.

Figure 1-1. Jetson Nano Block Diagram

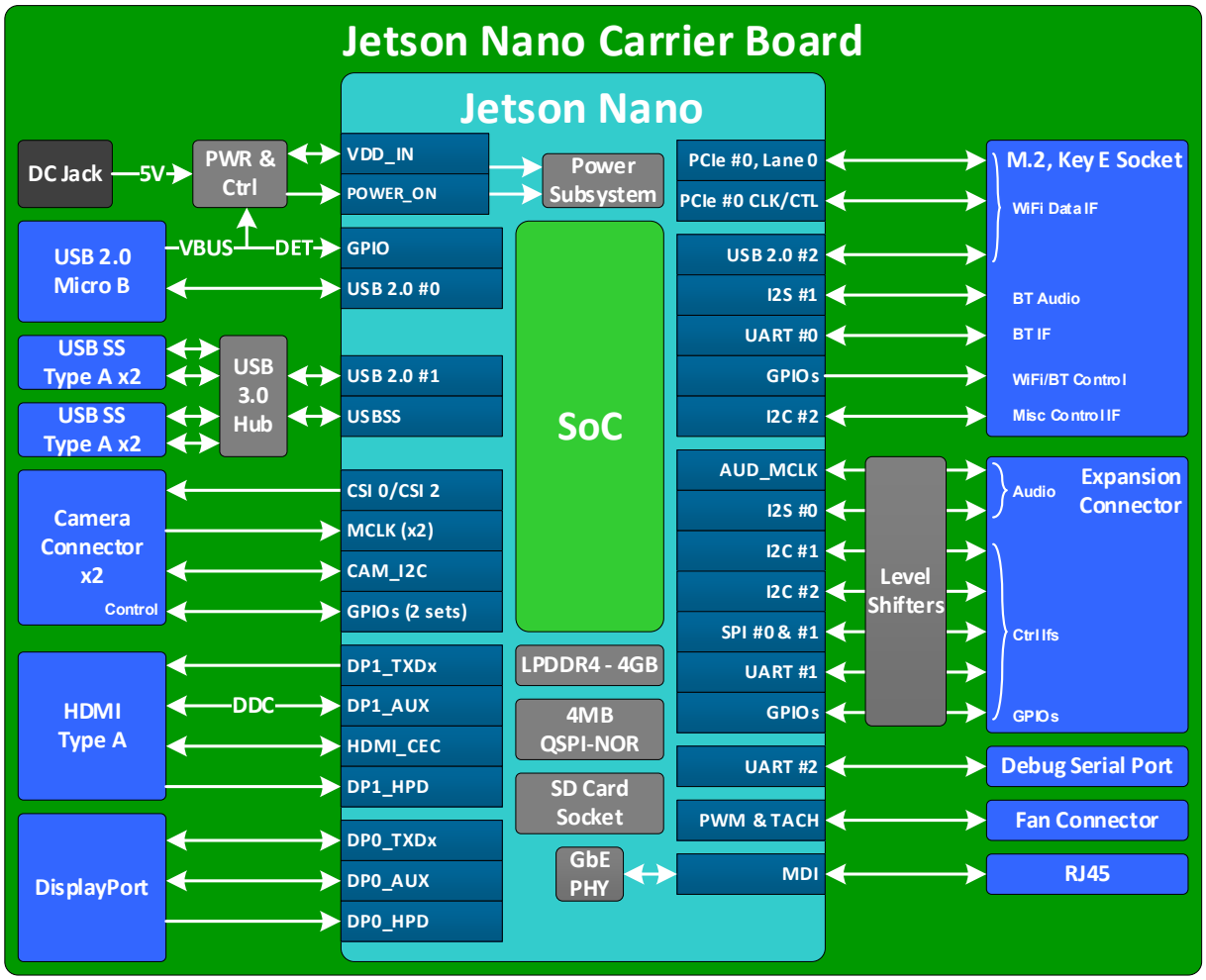


Figure 1-2. Jetson Nano Placement – Top View

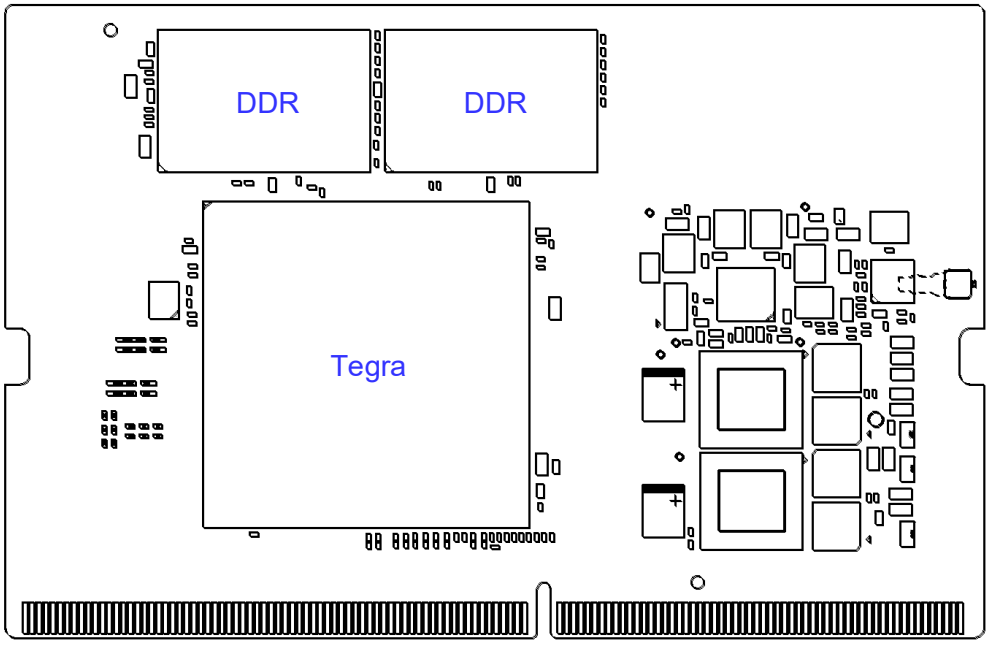


Figure 1-3. Jetson Nano Placement – Bottom View

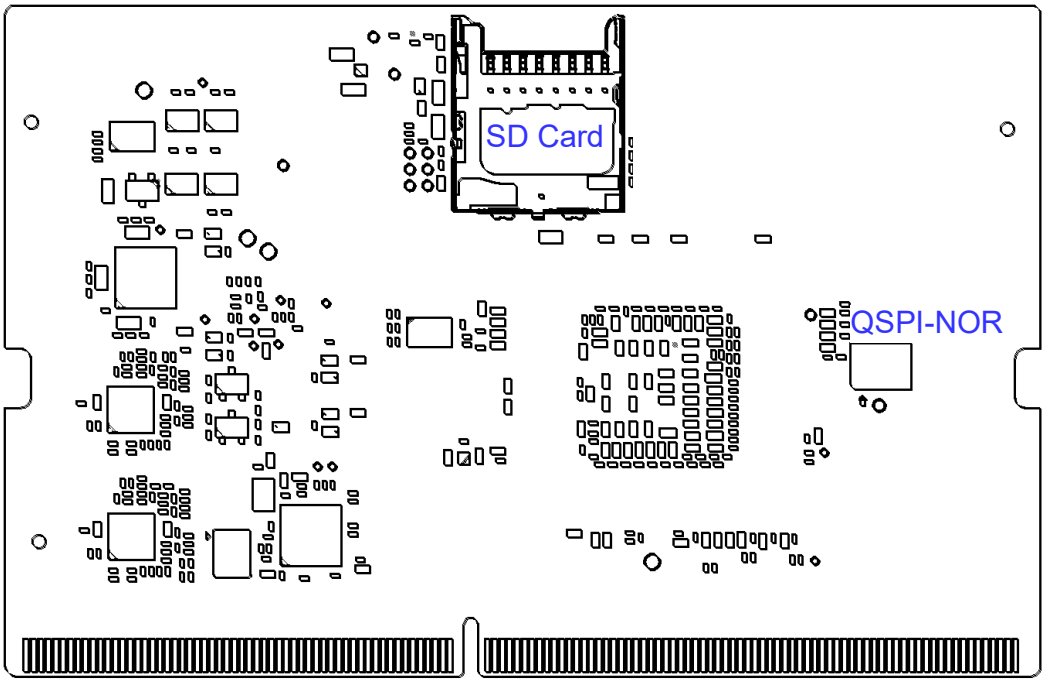
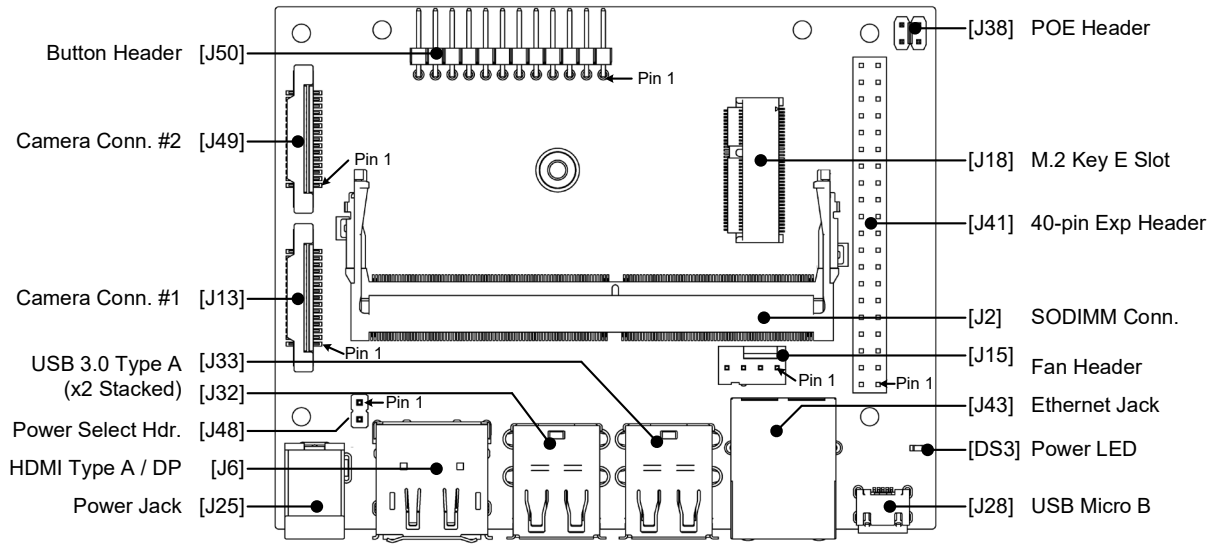
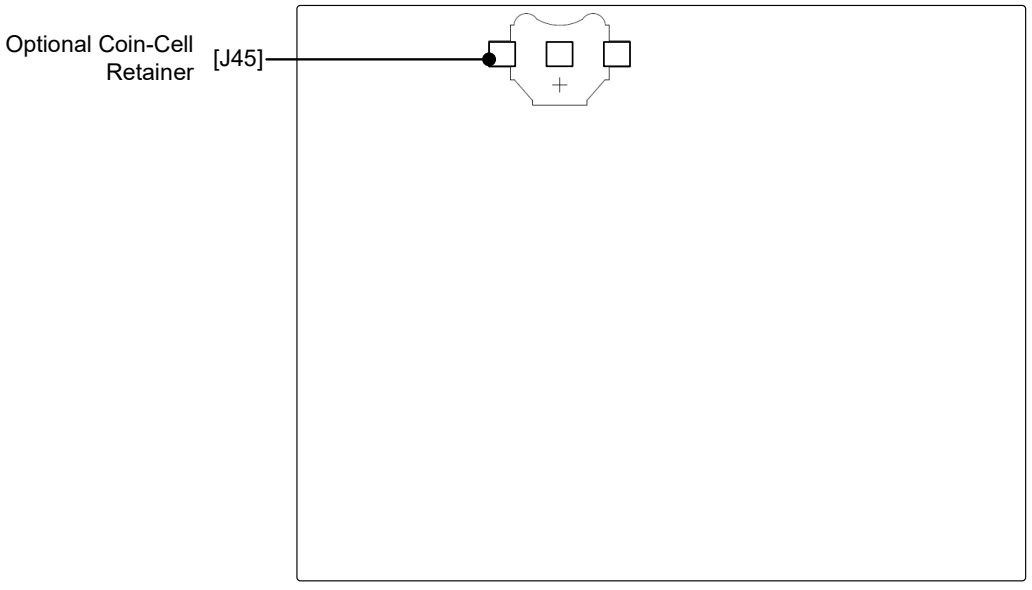


Figure 1-4. Jetson Nano Carrier Board Placement – Top View



J2 Jetson Nano Connector (SODIMM, 260-pin)
J6 HDMI Type A and DisplayPort Stacked Connector
J13 Camera (#1) Connector (15 pos, 1mm pitch)
J15 Fan Header (4-pin, 1.25mm pitch)
J18 M.2 Key E Socket (67-pin, 0.5mm pitch, RA)
J25 Power Jack
J28 USB Micro B, 5 position, 0.65mm pitch, RA Female
J32 USB Type A Dual Stacked Connector
J33 USB Type A Dual Stacked Connector
J38 Power-On-Ethernet Header (2x2, 2.54mm pitch)
J41 Expansion Header (2x20, 2.54mm pitch)
J43 RJ45 Ethernet Socket, 18-pins, RA, Female
J48 Power Jack/USB Power Select Jumper (1x2, 2.54mm pitch)
J49 Camera (#2) Connector (15 pos, 1mm pitch)
J50 Automation Header (1x12, 2.54mm pitch, RA)
DS3 Power LED (Green)

Figure 1-5. Jetson Nano Carrier Board Placement – Bottom View



J45 RTC Battery Back-up Coin Cell Retainer (Optional)

Chapter 2. Jetson Nano Carrier Board Standard Connectors

The Jetson Nano carrier board provides several connectors with industry standard pinouts to support additional functionality beyond what is integrated on the main platform board. This includes:

- USB 2.0: Micro B Connector
- USB 3.0: 2 x Type A Stacked Connectors
- Gigabit Ethernet: RJ45 Connector
- HDMI / DP: HDMI Type A and DisplayPort Stacked Connector
- M.2, Key E Socket
- Optional RCT Battery Back-up Coin Cell Retainer

2.1 USB Ports

The carrier board supports two USB Connectors. One is a USB 2.0 Micro B connector (J28) supporting Device mode only (including USB Recovery). There are two, dual stacked USB 3.0 Type A connectors (J32 and J33). Each connector supports Host mode only. A single load switch supplies VBUS to all four USB 3.0 ports and is limited to 2A of output current.

Table 2-1. USB 2.0 Micro B Connector Pin Description - J28

Pin #	Module Pin Name	Usage and Description	Type/Dir
1	–	VBUS Supply	Power
2	USB0_D_N	USB 2.0 #0 Data	Bidir
3	USB0_D_P		
4	–	Unused	Unused
5	–	Ground	Ground

Table 2-2. USB 3.0 Type A Connector Pin Description – J32

Pin #	Module Pin Name[1]	Usage/Description	Type/Dir[2]
USB 3.0 Type A (2)			
1	–	VBUS Supply	Power
2	USB1_D_N	USB 2.0 #2 Data from hub	Bidir
3	USB1_D_P		
4	–	Ground	Ground
5	USBSS_RX_N	USB 3.0 Receive #2 Data from hub	Input
6	USBSS_RX_P		
7	–	Ground	Ground
8	USBSS_TX_N	USB 3.0 Transmit #2 Data from hub	Output
9	USBSS_TX_P		
USB 3.0 Type A (1)			
10	–	VBUS Supply	Power
11	USB1_D_N	USB 2.0 Data #1 Data from hub	Bidir
12	USB1_D_P		
13	–	Ground	Ground
14	USBSS_RX_N	USB 3.0 Receive #1 Data from hub	Input
15	USBSS_RX_P		
16	–	Ground	Ground
17	USBSS_TX_N	USB 3.0 Transmit #1 Data from hub	Output
18	USBSS_TX_P		

Notes:

[1]The module pin names not directly connected to the USB connector pins but are routed to the input of the USB hub.

[2]In the Type/Dir column, Output is to USB Connectors. Input is from USB Connectors. Bidir is for Bidirectional signals.

Table 2-3. USB 3.0 Type A Connector Pin Description – J33

Pin #	Module Pin Name	Usage/Description	Type/Dir
USB 3.0 Type A (2)			
1	–	VBUS Supply	Power
2	USB1_D_N	USB 2.0 #4 Data from hub	Bidir
3	USB1_D_P		
4	–	Ground	Ground
5	USBSS_RX_N	USB 3.0 Receive #4 Data from hub	Input
6	USBSS_RX_P		
7	–	Ground	Ground
8	USBSS_TX_N	USB 3.0 Transmit #4 Data from hub	Output
9	USBSS_TX_P		
USB 3.0 Type A (1)			
10	–	VBUS Supply	Power
11	USB1_D_N	USB 2.0 Data #3 Data from hub	Bidir
12	USB1_D_P		
13	–	Ground	Ground
14	USBSS_RX_N	USB 3.0 Receive #3 Data from hub	Input
15	USBSS_RX_P		
16	–	Ground	Ground
17	USBSS_TX_N	USB 3.0 Transmit #3 Data from hub	Output
18	USBSS_TX_P		

Note: In the Type/Dir column, Output is to USB connectors. Input is from USB connectors. Bidir is for bidirectional signals.

2.2 Gigabit Ethernet

The carrier board implements an RJ45 connector (J43) along with the necessary magnetics device.

Table 2-4. Ethernet RJ45 Connector Pin Description – J43

Pin #	Module Pin Name	Usage/Description	Type/Dir
1	GPE_MDI0_P	Gigabit Ethernet MDI 0+	Bidir
2	GPE_MDI0_N	Gigabit Ethernet MDI 0–	Bidir
3	GPE_MDI1_P	Gigabit Ethernet MDI 1+	Bidir

Pin #	Module Pin Name	Usage/Description	Type/Dir
4	–	MCT	–
5	–	MCT	–
6	GPE_MDI1_N	Gigabit Ethernet MDI 1–	Bidir
7	GPE_MDI2_P	Gigabit Ethernet MDI 2+	Bidir
8	GPE_MDI2_N	Gigabit Ethernet MDI 2–	Bidir
9	GPE_MDI3_P	Gigabit Ethernet MDI 3+	Bidir
10	GPE_MDI3_N	Gigabit Ethernet MDI 3–	Bidir
11	–	Power-Over-Ethernet	Power
12	–		
13	–		
14	–		
15	–	Green LED Anode	Input
16	GBE_LED_LINK	Green LED Cathode. On for 1000 Mbps link, off for 10/100 Mbps link.	Output
17	–	Yellow LED Anode	Input
18	GBE_LED_ACT	Yellow LED Cathode. On indicates networking activity.	Output
19	–	Shield Ground	Ground
20	–	Shield Ground	Ground

Note: In the Type/Dir column, Output is to RJ45 connector. Input is from RJ45 connector. Bidir is for bidirectional signals.

2.3 HDMI and DisplayPort

A stacked DisplayPort (DP) and HDMI Type A connector (J6) is supported.

Table 2-5. HDMI Connector Pinout Description – J6

Pin #	Module Pin Name	Usage/Description	Type/Dir
1	DP1_TXD2_P	HDMI Transmit Data 2+	Output
2	–	Ground	Ground
3	DP1_TXD2_N	HDMI Transmit Data 2–	Output
4	DP1_TXD1_P	HDMI Transmit Data 1+	Output
5	–	Ground	Ground
6	DP1_TXD1_N	HDMI Transmit Data 1–	Output
7	DP1_TXD0_P	HDMI Transmit Data 0+	Output
8	–	Ground	Ground

Pin #	Module Pin Name	Usage/Description	Type/Dir
9	DP1_TXD0_N	HDMI Transmit Data 0–	Output
10	DP1_TXD3_P	HDMI Transmit Clock+	Output
11	–	Ground	Ground
12	DP1_TXD3_N	HDMI Transmit Clock–	Output
13	HDMI_CEC	HDMI CEC	Bidir
14	–	Unused	Unused
15	DP1_AUX_P	HDMI DDC Clock	Output /OD
16	DP1_AUX_N	HDMI DDC Data	Bidir/OD
17	–	Ground	Ground
18	–	HDMI 5V Power	Power
19	DP1_HPD	HDMI Hot Plug Detect	Input

Note: In the Type/Dir column, Output is to HDMI connector. Input is from HDMI connector. Bidir is for bidirectional signals.

Table 2-6. DP Connector Pin Description – J6

Pin #	Module Pin Name	Usage/Description	Type/Dir
1	DP0_TXD0_P	DP Lane 0+	Output
2	–	Ground	Ground
3	DP0_TXD0_N	DP Lane 0–	Output
4	DP0_TXD1_P	DP Lane 1+	Output
5	–	Ground	Ground
6	DP0_TXD1_N	DP Lane 1–	Output
7	DP0_TXD2_P	DP Lane 2+	Output
8	–	Ground	Ground
9	DP0_TXD2_N	DP Lane 2–	Output
10	DP0_TXD3_P	DP Lane 3+	Output
11	–	Ground	Ground
12	DP0_TXD3_N	DP Lane 3–	Output
13	–	MODE: Not used – pulled to GND through 1Mohm resistor	Unused
14	–	CEC_DP: Not used – pulled to GND through 1Mohm resistor	Unused
15	DP0_AUX_N	Display Port Auxiliary Channel 0-	Bidir
16	–	Ground	Ground
17	DP0_AUX_P	Display Port Auxiliary Channel 0+	Bidir
18	DP0_HPD	HDMI Hot Plug Detect	Input

Pin #	Module Pin Name	Usage/Description	Type/Dir
19	–	Power Return (Ground)	Ground
20	–	+3.3V	Power

Note: In the Type/Dir column, Output is to DP connector. Input is from DP connector. Bidir is for bidirectional signals

2.4 M.2, Key E Expansion Slot

The Jetson Nano carrier board includes an M.2, Key E Slot Mini-PCIe Expansion slot (J18). This includes interface options for WiFi/BT including PCIe (x1), USB 2.0, UART, I2S and I2C.

Table 2-7. M2, Key E Expansion Slot Pin Description – J18

Pin #	Module Pin Name	Usage/Description	Type/Dir	Pin #	Module Pin Name	Usage/Description	Type/Dir
1	–	Ground	Ground		–	–	–
3	USB2_D_P	USB 2.0 Data	Bidir	2	–	Main 3.3V Supply	Power
5	USB2_D_N			4			
7	–	Ground	Ground	6	–	Unused	Unused
9	–	Unused	Unused	8	I2S1_CLK	I2S #1 Clock	Bidir
11				10	I2S1_FS	I2S #1 Left/Right Clock	Bidir
13				12	I2S1_DIN	I2S #1 Data In	Input
15				14	I2S1_DOUT	I2S #1 Data Out	Bidir
17				16	–	Unused	Unused
19				18	–	Ground	Ground
21				20	GPIO2	Bluetooth Wake AP	Input
23				22	UART0_RXD	UART #0 Receive	Input
25	–	Key	Unused	24	–	Key	Unused
27				26			
29				28			
31				30			
33	–	Ground	Ground	32	UART0_TXD	UART #0 Transmit	Output
35	PEX0_TX0_P	PCIe #0 Transmit Lane 0	Output	34	UART0_CTS*	UART #0 Clear to Send	Input
37	PEX0_TX0_N			36	UART0_RTS*	UART #0 Request to Send	Output
39	–	Ground	Ground	38	–	Unused	Unused
41	PEX0_RX0_P	PCIe #0 Receive Lane 0	Input	40			
43	PEX0_RX0_N			42			
45	–	Ground	Ground	44			
47	PEX0_CLK_P	PCIe #0 Reference clock	Output	46			

Pin #	Module Pin Name	Usage/Description	Type/Dir	Pin #	Module Pin Name	Usage/Description	Type/Dir
49	PEX0_CLK_N			48			
51	–	Ground	Ground	50	CLK_32K_OUT	Suspend Clock (32KHz)	Output
53	PEX0_CLKREQ*	PCIe #0 Clock Request	Bidir	52	PEX0_RST*	PCIe #0 Reset	Output
55	PEX_WAKE*	PCIe Wake	Input	54	–	Unused	Unused
57	–	Ground	Ground	56			
59	–	Unused	Unused	58	I2C2_SDA	I2C #2	Bidir/OD
61				60	I2C2_SCL	I2C #2	Bidir/OD
63	–	Ground	Ground	62	GPIO10	M.2, Key E Connector Alert	Input
65	–	Unused	Unused	64	–	Unused	Unused
67				66			
69	–	Ground	Ground	68			
71	–	Unused	Unused	70			
73				72	–	Main 3.3V Supply	Power
75	–	Ground	Ground	74			

Note: In the Type/Dir column, Output is to M.2 module. Input is from M.2 module. Bidir is for bidirectional signals.

2.5 Real Time Clock Backup Coin-Cell Retainer Optional

The Jetson Nano carrier board includes pads on the bottom of the board to solder a coin-cell battery retainer (J45). The retainer is a 3000 type which accepts 12.5 mm x 2.5 mm, 3V coin cells such as the CR1225 (Lithium). If a non-rechargeable coin-cell is used, the charging circuit should be disabled before the battery is installed.

Table 2-8. RTC Battery Backup Coin-Cell Retainer Pin Description – J45

Pin #	Module Pin Name	Usage/Description	Type/Dir Default
1	PMIC_BBAT	RTC Back-up battery power	Power
2	–	Ground	Ground
3	PMIC_BBAT	RTC Back-up battery power	Power

Chapter 3. Carrier Board Custom Expansion Connecters

The Jetson Nano carrier board supports several expansion headers and connectors that have custom pinouts. These include the following:

- Jetson Nano module connector
  - 260-pin
  - SO-DIMM
  - 1.27 mm pitch
- Camera connectors (x2)
  - 15 position
  - Flex connector
  - 0.5 mm pitch
- Expansion header
  - 2x20
  - 2.54 mm pitch
- Automation header
  - 2x4
  - 2.54 mm pitch
- Fan connector
  - 4-pin
  - 1.25 mm pitch
- DC power jack

3.1 Jetson Nano Module Connector

The carrier board interfaces to the Jetson Nano module using a 260-pin SODIMM connector (J2). The carrier board has a TE Connectivity 2309413-1 connector. This interfaces with the Jetson Nano edge fingers. The connector pinout can be found in the *Jetson Nano Product Design Guide*.

3.2 Camera Connector

The Jetson Nano carrier board includes two 15-position flex (0.5mm pitch) camera connectors (J13 and J49). The connector used on the carrier board is a TE Connectivity Part #1-1734248-5. Each connector includes:

- CSI 1 x2 lane
- CAM_I2C, Clock and Control GPIOs for the camera
- 3.3V Supply

Note: In the Type/Dir column in Table 3-1 and Table 3-2 Output is to Camera module. Input is from Camera module. Bidir is for bidirectional signals.

Table 3-1. Camera #1 Connector Pin Description – J13

Pin #	Module Pin Name	Usage/Description	Type/Dir	Pin #	Module Pin Name	Usage/Description	Type/Dir
1	–	Ground	Ground	2	–	Not Used	–
3	CSI_0_D0_N	CSI 0 Data 0	Input	4	–		
5	CSI_0_D0_P			6	–		
7	–	Ground	Ground	8	–		
9	CSI_0_D1_N	CSI 0 Data 1	Input	10	–		
11	CSI_0_D1_P			12	–		
13	–	Ground	Ground	14	–		
15	CSI_0_CLK_N	CSI 0 Clock	Input	16	–		
17	CSI_0_CLK_P			18	–		
19	–	Ground	Ground	20	–		
21	CAM0_PWDN	Camera #0 Power-down	Output	22	–		
23	CAM0_MCLK	Camera #0 Master Clock	Output	24	–		
25	CAM_I2C_SCL	Camera I2C. 2.2kΩ pull-ups on module. 1.6kΩ pull-ups on the carrier board. The module CAM_I2C pins connect to an I2C mux. The camera connector #1 receives the I2C from the mux (1st output)	Output	26	–		
27	CAM_I2C_SDA		Bidir	28	–		
29	–	+3.3V	Power	30	–		

Table 3-2. Camera #2 Connector Pin Description – J49

Pin #	Module Pin Name	Usage/Description	Type/Dir	Pin #	Module Pin Name	Usage/Description	Type/Dir
1	–	Ground	Ground	2	–	Not Used	–
3	CSI_2_D0_N	CSI 2 Data 0	Input	4	–		
5	CSI_2_D0_P			6	–		
7	–	Ground	Ground	8	–		
9	CSI_2_D1_N	CSI 2 Data 1	Input	10	–		
11	CSI_2_D1_P			12	–		
13	–	Ground	Ground	14	–		
15	CSI_2_CLK_N	CSI 2 Clock	Input	16	–		
17	CSI_2_CLK_P			18	–		
19	–	Ground	Ground	20	–		
21	CAM1_PWDN	Camera #1 Power-down	Output	22	–		
23	CAM1_MCLK	Camera #1 Master Clock	Output	24	–		
25	CAM_I2C_SCL	Camera I2C. 2.2kΩ pull-ups on module. 1.6kΩ pull-ups on the carrier board. The module CAM_I2C pins connect to an I2C mux. The camera connector #2 receives the I2C from the mux (2nd output)	Output	26	–		
27	CAM_I2C_SDA		Bidir	28	–		
29	–	+3.3V	Power	30	–		

3.3 40-Pin Expansion Header

The Jetson Nano carrier board includes a 40-pin (2x20, 2.54 mm pitch) Expansion Header (J41). The connector used on the carrier board is an Astron Technology (Part # 27-0169H-220-1G-H). The expansion connector includes various audio and control interfaces including:

- I2S
- Audio Clock
- I2C (x2)
- SPI (x2)
- UART
- GPIOs (x3 – See Note)

Notes:

- All the signals on the expansion header use 3.3V levels.
- All the interface signal pins (I2S, I2C, SPI, UART and Audio clock) can also be configured as GPIOs
- Any pull-up or pull-down resistors on the signals (except I2C) must be weak (limited to >50kΩ).

Figure 3-1. Expansion Header Connections

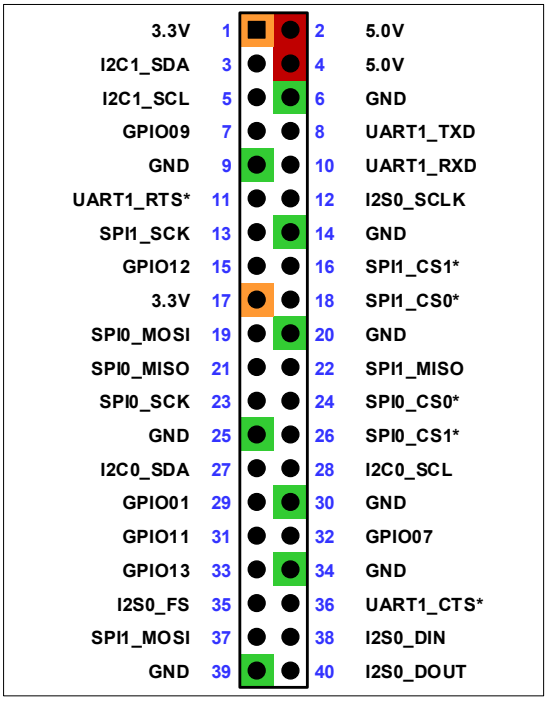


Table 3-3. Expansion Header Pin Description – J41

Header Pin #	Module Pin Name	Module Pin #	Tegra Pin name	Default Usage / Description	Alternate Functionality	Type/ Direction	Pin Drive or Power Pin Max Current	Tegra GPIO Port #	Power-on Default	PU/PD on Module	Notes
1	–	–	–	Main 3.3V Supply	–	Power (input)	1A	–	–	–	1
2	–	–	–	Main 5.0V Supply	–	Power (input/output_	1A	–	–	–	1
3	I2C1_SDA	191	GEN2_I2C_SDA	I2C #1 Data	GPIO	Bidir/OD	1mA / -1mA	PJ.03	z	2.2KΩ PU	2
4	–	–	–	Main 5.0V Supply	–	Power	1A	–	–	–	–
5	I2C1_SCL	189	GEN2_I2C_SCL	I2C #1 Clock	GPIO	Bidir/OD	1mA / -1mA	PJ.02	z	2.2KΩ PU	2
6	–	–	–	Ground	–	Ground	–	–	–	–	–
7	GPIO09	211	AUD_MCLK	GPIO	Audio Master Clock	Bidir/Output	20uA / -20uA	PBB.00	pd		3
8	UART1_TXD	203	UART2_TXD	UART #1 Transmit	GPIO	Bidir/Output	20uA / -20uA	PG.00	pd		3
9	–	–	–	Ground	–	Ground	–	–	–	–	–
10	UART1_RXD	205	UART2_RXD	UART #1 Receive	GPIO	Bidir/Input	20uA / -20uA	PG.01	pu		3
11	UART1_RTS*	207	UART2_RTS	GPIO	UART #2 Request to Send	Bidir/Output	20uA / -20uA	PG.02	pd		3
12	I2S0_SCLK	199	DAP4_SCLK	GPIO	Audio I2S #0 Clock	Bidir	20uA / -20uA	PJ.07	pd		3
13	SPI1_SCK	106	SPI2_SCK	GPIO	SPI #1 Shift Clock	Bidir/Output	20uA / -20uA	PB.06	pd		3
14	–	–	–	Ground	–	Ground	–	–	–	–	–
15	GPIO12	218	LCD_TE	GPIO	–	Bidir	20uA / -20uA	PY.02	pd		3
16	SPI1_CSI1*	112	SPI2_CS1	GPIO	SPI #1 Chip Select #1	Bidir/Output	20uA / -20uA	PDD.00	pu		3
17	–	–	–	Main 3.3V Supply	–	Power	1A	–	–	–	1
18	SPI1_CSI0*	110	SPI2_CS0	GPIO	SPI #0 Chip Select #0	Bidir/Output	20uA / -20uA	PB.07	pu		3
19	SPI0_MOSI	89	SPI1_MOSI	GPIO	SPI #0 Master Out/Slave In	Bidir/Output	20uA / -20uA	PC.00	pd		3
20	–	–	–	Ground	–	Ground	–	–	–	–	–
21	SPI0_MISO	93	SPI1_MISO	GPIO	SPI #0 Master In/Slave Out	Bidir/Input	20uA / -20uA	PC.01	pd		3
22	SPI1_MISO	108	SPI2_MISO	GPIO	SPI #1 Master In/Slave Out	Bidir/Input	20uA / -20uA	PB.05	pd		3
23	SPI0_SCK	91	SPI1_SCK	GPIO	SPI #0 Shift Clock	Bidir/Output	20uA / -20uA	PC.02	pd		3
24	SPI0_CS0*	95	SPI1_CS0	GPIO	SPI #0 Chip Select #0	Bidir/Output	20uA / -20uA	PC.03	pu		3
25	–	–	–	Ground	–	Ground	–	–	–	–	–

Header Pin #	Module Pin Name	Module Pin #	Tegra Pin name	Default Usage / Description	Alternate Functionality	Type/ Direction	Pin Drive or Power Pin Max Current	Tegra GPIO Port #	Power-on Default	PU/PD on Module	Notes
26	SPI0_CS1*	97	SPI1_CS1	GPIO	SPI #0 Chip Select #1	Bidir/Output	20uA / -20uA	PC.01	pu		3
27	I2C0_SDA	187	GEN1_I2C_SDA	I2C #0 Data	GPIO	Bidir/OD	1mA / -1mA	PB.05	z	2.2KΩ PU	2
28	I2C0_SCL	185	GEN1_I2C_SCL	I2C #0 Clock	GPIO	Bidir/OD	1mA / -1mA	PC.02	z	2.2KΩ PU	2
29	GPIO01	118	CAM_AF_EN	GPIO	Camera MCLK #2	Bidir/Output	20uA / -20uA	PC.03	pd		3
30	–	–	–	Ground	–	Ground	–	–	–	–	–
31	GPIO11	216	GPIO_PZ0	GPIO	Camera MCLK #3	Bidir/Output	20uA / -20uA	PZ.00	pd		3
32	GPIO07	206	LCD_BL_PWM	GPIO	PWM	Bidir/Output	20uA / -20uA	PV.00	pd		3
33	GPIO13	228	GPIO_PE6	GPIO	PWM	Bidir/Output	20uA / -20uA	PE.06	pd		3
34	–	–	–	Ground	–	Ground	–	–	–	–	–
35	I2S0_FS	197	DAP4_FS	GPIO	Audio I2S #0 Field Select	Bidir	20uA / -20uA	PJ.04	pd		3
36	UART1_CTS*	209	UART2_CTS	GPIO	UART #1 Clear to Send	Bidir/Input	20uA / -20uA	PG.03	pd		3
37	SPI1_MOSI	104	SPI2_MOSI	GPIO	SPI #1 Master Out/Slave In	Bidir/Output	20uA / -20uA	PB.04	pd		3
38	I2S0_DIN	195	DAP4_DIN	GPIO	Audio I2S #0 Data in	Bidir/Input	20uA / -20uA	PJ.05	pd		3
39	–	–	–	Ground	–	Ground	–	–	–	–	–
40	I2S0_DOUT	193	DAP4_DOUT	GPIO	Audio I2S #0 Data Out	Bidir/Output	20uA / -20uA	PJ.06	pd		3

Notes:

1. This is current capability per power pin.
2. These pins are connected to NVIDIA® Tegra® directly. They are open-drain (either pulled up or driven low by Tegra when configured as outputs). The max drive that meets the data sheet VOL is 1 mA.
3. These pins connect to TI TXB0108 level translators. Due to the design of these devices, the output drivers are very weak, so they can be overdriven by another connected device output for bidirectional support.
4. In the Type/Dir column, output is to expansion header. Input is from expansion header. Bidir is for bidirectional signals. Where two directions are shown, the first is for the primary function (mostly GPIOs) and the second is for the alternate function.
5. Where the signal direction is input or output in Table 3-3, this matches the typical special function usage (e.g. SPI, I2S, etc.). The direction is bidirectional if these are configured as GPIOs.
6. All signals on the 40-pin header are 3.3V levels.

3.4 Automation Header

The Jetson Nano carrier board brings several system signals (power, reset, and force recovery), UART and Sleep/Wake LED related signals to a 12-pin standard 0.254 mm pitch right-angle header (J50).

Table 3-4. Automation Header Description – J50

Pin #	Signal Name	Module Pin Name	Usage/Description	Type/Dir Default
1	PC_LED-	-	Connects to LED Cathode to indicate System Sleep/Wake (Off when system in sleep mode)	Input
2	PC_LED+	-	Connects to LED Anode (see Pin 1)	Output
3	UART2_RXD_LS	UART2_RXD (DEBUG)	UART #2 Receive	Input
4	UART2_TXD_LS	UART1_TXD (DEBUG)	UART #2 Transmit	Output
5	LATCH_SET	–	Connect Pin 5 and Pin 6 to disable Auto-Power-On and require power automation press.	Input
6	LATCH_SET_BUT	–	See Pin 5.	Output
7	GND	–	Ground	Ground
8	SYS_RST*	SYS_RESET*	Temporarily connect Pin 7 and Pin 8 to reset system	Input

Pin #	Signal Name	Module Pin Name	Usage/Description	Type/Dir Default
9	GND	–	Ground	Ground
10	FORCE_RECOVERY*	FORCE_RECOVERY*	Connect Pin 9 and Pin 10 during power-on to put system in USB Force Recovery mode.	Input
11	GND	–	Ground	Ground
12	PWR_BTN*	SLEEP/WAKE*	Connect Pin 11 and Pin 12 to initiate power-on if Auto-Power-On disabled (Pin 5 and Pin 6 connected).	Input

Note: In the Type/Dir column, Output is to automation header. Input is from automation header. Bidir is for bidirectional signals.

3.5 Fan Connector

The Jetson Nano carrier board includes a 4-pin Fan Header (J15). The connector used is a Singatron Enterprise Co., Ltd., Part # 2WBA2542WVC-F-04PNLBT1N00G.

Table 3-5. Fan Connector Pin Description – J15

Pin #	Module Pin Name	Usage/Description	Type/Dir Default
1	–	Ground	Ground
2	–	Main 5.0V Supply	Power
3	GPIO8 (SDMMC_CD)	Fan Tachometer signal	Input
4	GPIO14 (PWM)	Fan Pulse Width Modulation signal	Output

Note: In the Type/Dir column, Output is to fan connector. Input is from fan connector. Bidir is for bidirectional signals.

3.6 DC Power Jack

The Jetson Nano carrier board uses a DC power jack (J25) to bring in the power from a DC power supply. Note that a jumper must be installed on (J48) to enable power input via the (J25) power jack. The jack used on the carrier board is a Singatron Enterprise part (Part #: 2DC-0005D200). The center pin is (+). The mating barrel jack connector dimensions are:

- Barrel length: 9.5 mm
- Barrel diameter:5.5 mm
- Pin receptacle: Accepts 2 mm jack pin
- The center pin is positive (+V)
- Max current supported is 4A

Figure 3-2. DC Power Jack Pin

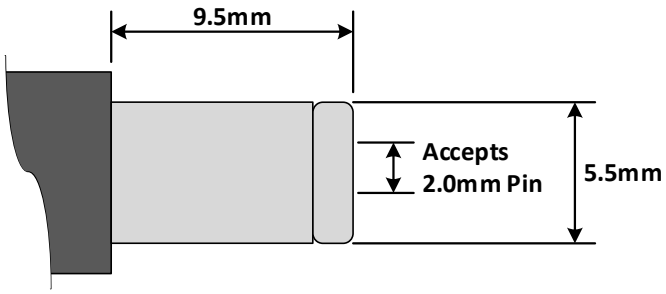


Table 3-6. DC Jack Pin Description – J25

Pin #	Module Pin Name	Usage/Description	Type/Dir Default
1	VDD_IN (see Note)	Main DC input supplying VDD_5V_IN/VDD_IN	Power
2	–	Ground	Ground
3	–	Ground	Ground

Note: VDD_DC_JACK connects to input of Power MUX. VDD_IN connects to output of that device.

Chapter 4. Mechanicals

Figure 4-1 and Figure 4-2 show the mechanical dimensions for the carrier board and the developer kit.

Figure 4-1. Developer Kit Carrier Board Mechanical Dimensions

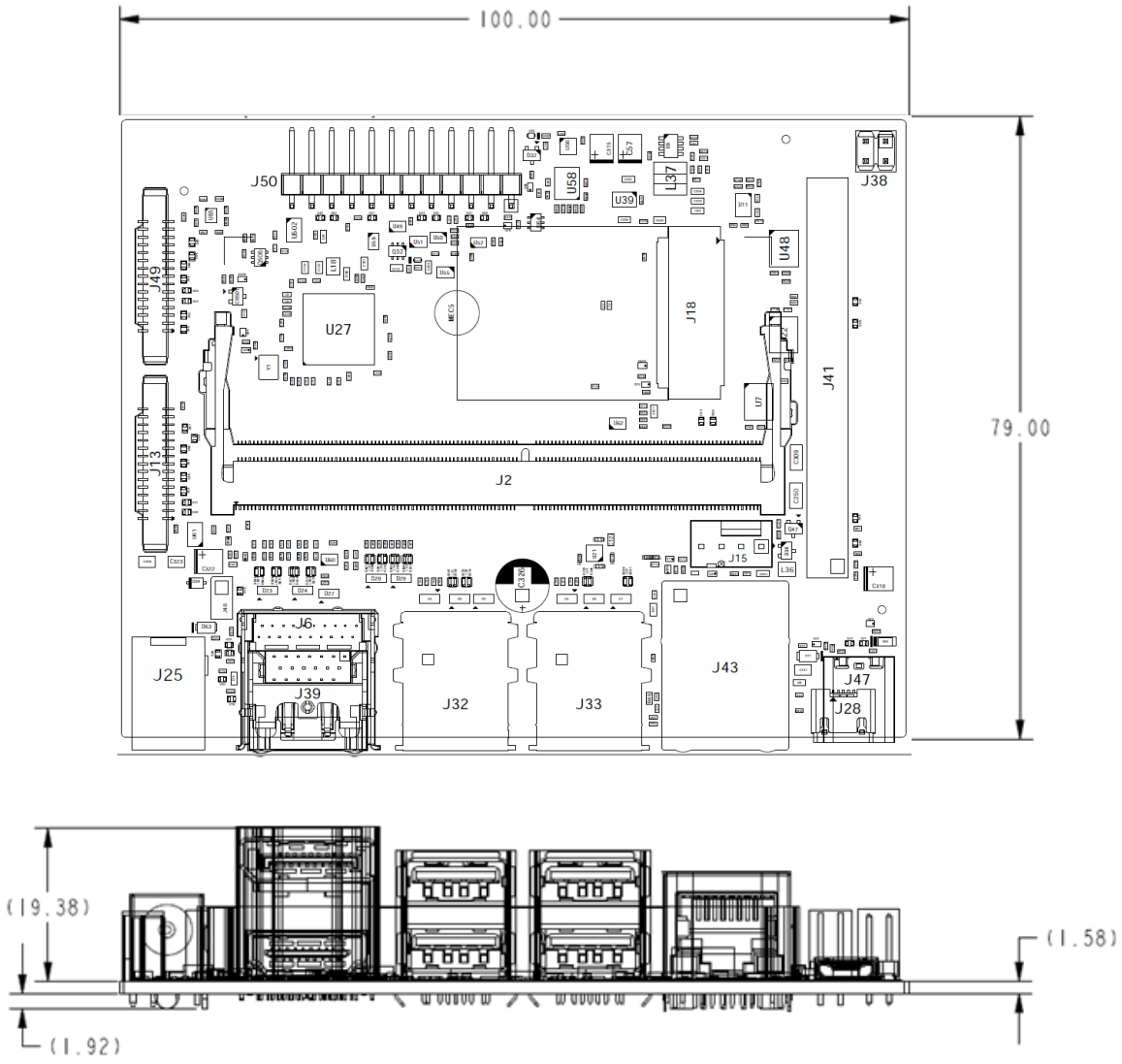
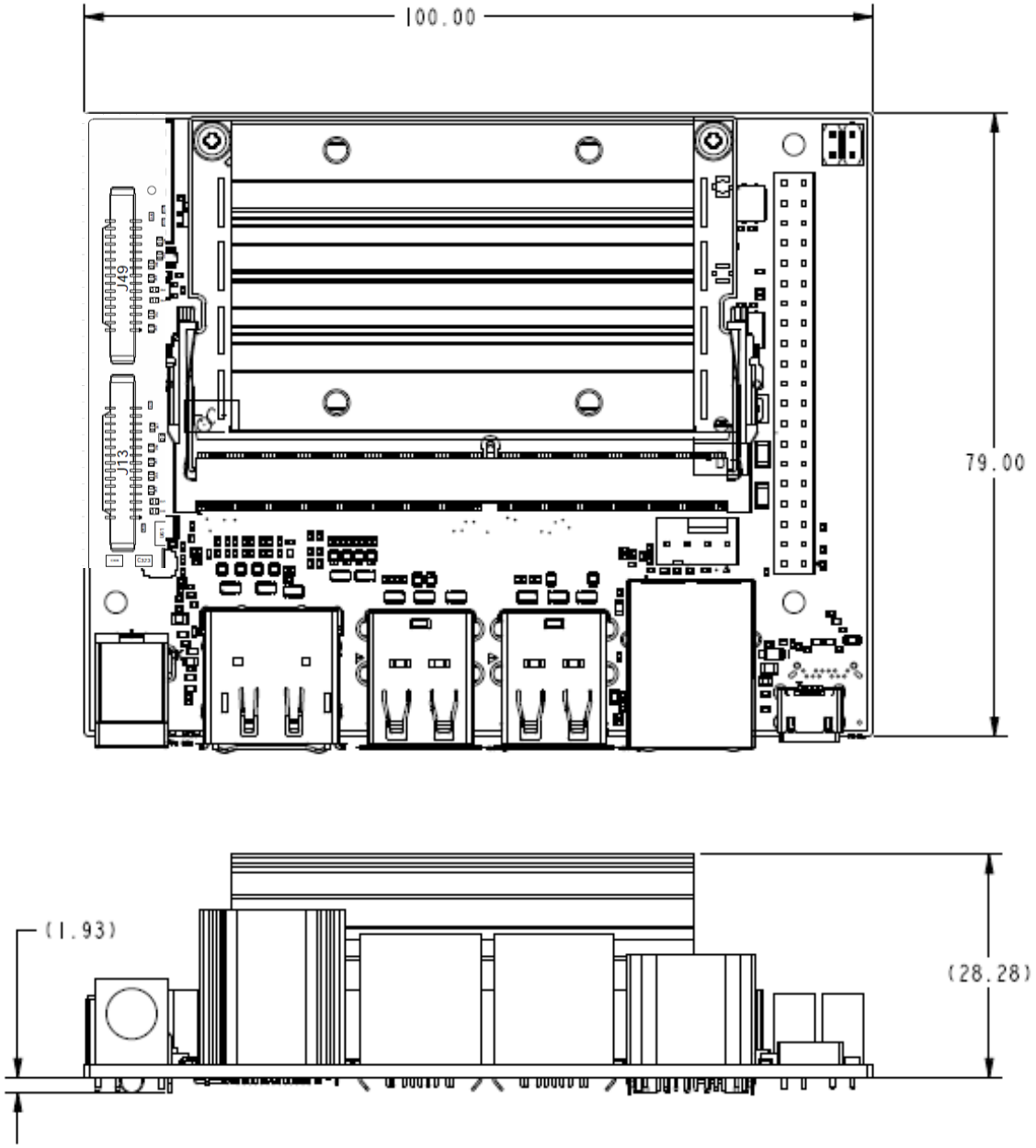


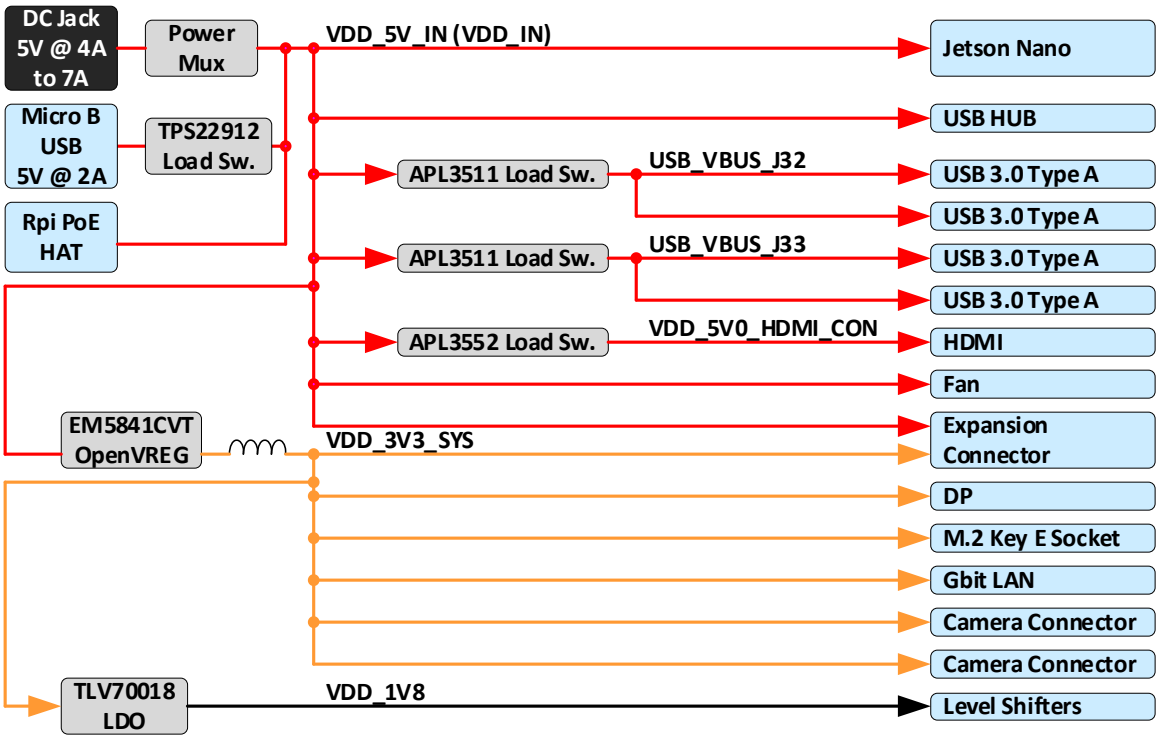
Figure 4-2. Developer Kit Mechanical Dimensions



Chapter 5. Interface Power

Figure 5-1 shows the interface connector power diagram.

Figure 5-1. Interface Connector Power Diagram



The following tables show the allocation of supplies to the connectors on the Jetson carrier board and current capabilities.

Table 5-1. Interface Power Supply Allocation

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable
VDD_5V_IN/VDD_INI	Main power input from DC Adapter	5.0	TPS25944L Power Mux	DC Adapter	J48 installed
VDD_5V_USB	5V power input from USB Micro B	5.0	TPS259530 Load Switch	Micro B Connector	J48 removed
VDD_3V3_SYS	Main 3.3V supply	3.3	MP1475	VDD_5V_IN	SYS_RESET_IN*
VDD_1V8	Main 1.8V supply	1.8	TVL70018 LDO	VDD_3V3_SYS	3.3V_IO_PG
USB_VBUS_J32	5V VBUS for dual stacked 3.0 Type A connector	5.0	TPS259530 Load Switch	VDD_5V_IN	From USB Hub
USB_VBUS_J33	5V VBUS for dual stacked 3.0 Type A connector	5.0	TPS259530 Load Switch	VDD_5V_IN	From USB Hub
VDD_5V0_HDMI_CON	5V rail for HDMI connector	5.0	APL3552 Load Switch	VDD_5V_IN	VDD_3V3_SYS

Table 5-2. Interface Supply Current Capabilities

Power Rails	Usage	(V)	Max Current (mA)
VDD_5V_IN/VDD_IN	Main power input from DC dapter	5.0	~DC Adapter: 4000 USB Micro B Charger: 2000
VDD_3V3_SYS	Main 3.3V supply	3.3	1500
VDD_1V8	Main 1.8V supply	1.8	100

Note: The DC jack circuit on the developer kit is rated only up to 4.0A.

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